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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,988	01/30/2004	Christian Peters	20196/0200688-US0	4530

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EXAMINER	
YOHA, CONNIE C	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,988	PETERS ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha
CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

Information Disclosure Statement (IDS) filed on 1/30/04 was considered.

2. Claims 1-7 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, with regard to claim 2, wherein the group of memory transistors has 16 to 32 memory transistors needs to shown in the drawings. With regard to claim 6, the means for measuring a first current flowing through each row or column to be read; means for storing the measured first current; means for supplying a read potential to gate terminals of the row or column to be read means for measuring a resulting second current flow through the row or column to be read; and means for comparing the second current with the stored first current, must all be shown in the drawings.

Claim Objections

4. Claim 5, 6, and 7 are objected to because of the following informalities: It is vague and not clear to the Examiner, if "opening the selection transistor" meaning to turn "off" or turn "on" the selection transistor. In the field of semiconductor memory, when a transistor is in an open state, it is meant to be in an "off" state or that the transistor is not conductive to transfer current to the selected data line or bitline. Thus,

when the selection transistor (fig. 1, element 3) is open (is in an "off" state"), then current I1 cannot be read out to be use in the comparison with the current I2. Therefore, in claim 5-7, applicant claimed "opening the selection transistor while gate terminals of the memory transistors of the group of the memory transistors are at low potential; measuring a first current flowing through each row or column to be read" is not well understood by the examiner. Please provide clarifications and corrections.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwahashi, Pat. No. 6081453.

With regard to claim 1, Iwahashi discloses a memory comprising: memory transistors (fig. 1, MC) arranged in a group (fig. 1, all memory MC connected to each of the BL) or (fig. 6, 11-1 through 11-8)); a drive circuit (fig. 1, 12) coupled to a memory transistor (fig. 1, MC) of the group so that information can be written to and read from the memory transistor; and a selection transistor (fig. 1, each transistor in element 14 connected to the BL) so that the group of the memory transistors can be jointly selected (col. 2, line 1-10).

With regard to claim 3, Iwahashi discloses wherein the group of memory transistors is arranged in at least one of a row and a column (fig. 1, all memory cells connected to the each BL is considered a group of memory transistors).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwahashi, Pat. No. 6081453 in view of Park et al, Pat. No. 6501684.

With regard to claim 2 and 4, Iwahashi, as applied in prior rejection, disclosed all claimed subject matter except wherein the group of memory transistors has 16 to 32 memory transistors. However, Park discloses a conventional memory array arranged in rows and columns, wherein each group of memory has 16 to 32 memory transistors (col. 6, line 36-38) forming a data bytes that is individually accessible and can be program, read and erased. It would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate the memory structures of Park's into Iwahashi's to achieve a 16 or a 32 bytes of data for each data group to form a memory which is 16-bits or 32 bits wide.

cited for the same reason as set forth above.

Allowable Subject Matter

7. Claim 5-7 are objected, but would be allowable if rewritten to overcome all the objection set forth above.

The prior art of record does not show the limitation of memory device and method of having in combination with other features; a means for opening the selection transistor while gate terminals of the memory transistors of the group of memory transistors are al low potential; means for measuring a first current flowing through each row or column to be read; means for storing the measured first current ; means for supplying a read potential to gate terminals of the row or columns to be read; means for measuring a resulting second current flowing through the row or column to be read ;and means for comparing the second current with the stored first current.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Kunori et al (6144584), Jang (6044033), Poplevine et al (6563730) and Andoh et al (5182725) disclose a memory device.

9. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

November 2004

CONNIE C. YOHA
PRIMARY EXAMINER